REMARKS

For the reasons set forth in detail below, applicant submits that the present application, including each of the pending claims, is in condition for allowance. In the non-final Office Action mailed on November 15, 2005, the Examiner rejected claims 1-13. In particular:

claims 1-13 are provisionally rejected on the ground of nonstatutory double patenting; and

claims 1-13 are rejected under 35 U.S.C. § 103(a).

In this response claims 1-13 remain pending.

Rejection Under Nonstatutory Obviousness-Type Double Patenting of Claims 1-13

In the Office Action, claims 1-13 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-15 of the applicant's copending Application No. 10/772,159 and also over claims 1-3, 5, 7, and 8 of the applicant's copending Application No. 10/625,411.

Without conceding to the Examiner's assertion that claims 1-13 are obvious variations of the above mentioned claims in U.S. Patent Application No. 10/772,159 and U.S. Patent Application No. 10/625,411, the undersigned has enclosed herewith a terminal disclaimer to expedite prosecution. In light of the enclosed terminal disclaimer, the obviousness-type double patenting rejection of claims 1-13 should be withdrawn.

Rejection Under 35 U.S.C. § 103(a) of Claims 1-13

The Examiner rejected claims 1-13 under 35 U.S.C. § 103(a) as being unpatentable over Chung et al (US Pat. No. 6,218,691).

Chung, as the Examiner has reiterated in page 4 of the Office Action, discloses what the applicant has already mentioned in his background section as inefficient prior art. Specifically, Chung teaches a plurality of unit pixels each including a pinned photodiode, a transfer transistor connected between the photodiode and an output node, a reset transistor connected between a voltage reference and the output node, an output transistor coupled to the output node, and a selection transistor connected between the output transistor and an output circuitry.

The problem Chung tries to solve, which is stated in his background section in col. 2, lines 5-8, is that "since the conventional unit pixel may not increase the voltage variation range, the dynamic range of the output terminal of the unit pixel is substantially limited." Chung is merely concerned about improving the dynamic range of the output of his image sensor. In col. 2, lines 12-14 Chung states his objection as: "to provide an image sensor that is characterized by an improved output dynamic range and respectable charge transfer and quantum efficiencies". The only image sensor circuit Chung discloses is the one of Figure 3, which has been mentioned as prior art in the present invention. As evident from col. 2, lines 46-55, Chung is only concerned about the voltages applied to this circuit.

Another indication that Chung is not concerned with reducing the amount of circuitry in an array of pixels is that he mentions once an array of pixels, and that is when he provides fabrication advice. Regarding an array of pixels, in col. 3, lines 36-45, Chung merely states:

> "The unit pixel array is divided by the N-type buried layer and a negative voltage is applied to the divided unit pixel array. At this time, field oxide layers are formed between the unit pixels and the unit pixels should be isolated from the peripheral circuit by the N-type buried layer. The P-epi layer of the unit pixel is surrounded by the N-type buried layer so that the P-epi layer of the unit pixel is isolated from the P-epi layer of the peripheral circuit, and independently receives a negative voltage."

In summary, Chung has not disclosed, taught, suggested, or even implied the sharing of transistors to reduce silicon real estate and/or power consumption of image sensor arrays/systems.

In contrast, the independent claims 1 and 8 of the present application, *inter alia*, are directed to multiple pixels sharing a single reset transistor and a single output transistor, without the need for selection transistors. For example claim 8 recites:

> "a plurality of pixels arranged in rows and columns formed in a semiconductor substrate...a plurality of output nodes, each of said output nodes shared between at least two of said pixels and for receiving said signal from said at least two of said pixels...a plurality of output transistors associated with said plurality of output nodes, each of said output transistors shared between said at least two of said pixels". (Emphasis added)

The claimed transistor-sharing decreases the number of transistors to as low as about 40% of number of transistors of prior art. Among other advantages, this significantly reduces silicon real estate and power consumption of image sensor systems. However, the Examiner states that it is obvious to one of ordinary skill in the imaging art to share the above mentioned transistors.

The saving of silicon real estate and power are two primary goals of every single chip designer. However, this claimed sharing of transistors is not disclosed in any cited prior art. The Examiner is respectfully requested to cite to prior art how such sharing of transistors can be obvious.

According to MPEP 2142: The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

To reach a proper determination under 35 USC 103, the examiner must step backward in time and into the shoes worn by the hypothetical "person of ordinary skill in

the art" when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention "as a whole" would have been obvious at that time to that person. Knowledge of applicant's disclosure must be put aside in reaching this determination, yet kept in mind in order to determine the "differences," conduct the search and evaluate the "subject matter as a whole" of the invention. The tendency to resort to "hindsight" based upon applicant"s disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art. See MPEP 2142.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. See MPEP 2143.

Again, according to MPEP 2144: The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

The undersigned maintains that a *prima facie* case of obviousness under 35 U.S.C. § 103 has not been established with respect to the independent claims 1 and 8 and, accordingly, the Section 103 rejection of these claims should be withdrawn.

Claims 2-7 and 9-13 depend from independent claims 1 and 8, respectively, and include the features of these independent claims. For reasons discussed above and for the additional features of these claims a *prima facie* case of anticipation under Section 103 has not been established with respect to these dependent claims and accordingly the undersigned requests their allowance.

Conclusion

In view of the foregoing, all of the claims pending in the application are in condition for allowance and, therefore, a Notice of Allowance is respectfully requested. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206) 359-6488.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 384938068US from which the undersigned is authorized to draw.

Dated: 2/7/06

Respectfully submitted,

By _____

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